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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,207	04/02/2004	Kenneth S. Goekjian	A2004003	2438

26643 7590 10/12/2006

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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,207	GOEKJIAN ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

10/5/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

Applicant's arguments filed 08/07/2006 have been fully considered but they are not persuasive.

The applicant discloses "With reference to FIG. 1, Kabenjian discloses an architecture for independent data transfers on a single, shared port, "primary I/O interface 150", and it is the optimal use of I/O bus 152 with which Kabenjian appears primarily concerned. Primary interface 150 represents a conventional I/O interface, rather than a plurality of ports, as that term is understood in the art".

This statement is true; however, Kabenjian discloses the devices (the controllers), as discloses in col. 8, lines 52-60, having their own I/O access points (see fig. 1). In another word, each of these devices have they own ports. See col. 5, lines 61-63 and col. 8, lines 45-60.

The applicant's invention discloses the ports having their own FIFO and channel; similar, Kabenjian discloses (col. 8, lines 45-60 discloses "The DMA unit 200 of the preferred embodiment has four independent DMA channels. A first DMA channel comprises the first register block 300 and the first data buffer 252. A second DMA channel comprises the second register block 320 and the second data buffer 254. A third DMA channel comprises the third register block 340 and the third data buffer 256. A fourth DMA channel comprises the fourth register block 360 and the fourth data buffer 258. Each DMA channel in the DMA unit 200 is preferably used for DMA transfers with a particular I/O device or a particular group of I/O devices. For example, the first DMA

channel may be used with the IDE controller 154, the second DMA channel may be used with the graphics controller 160, the third DMA channel may be used with the SCSI controller 162, and the fourth DMA channel may be used with the LAN controller 166").

The applicant's claims did not disclose the FIFOs connected to the devices; in other word, being on the devices' side.

In regards to claim 2-6, similar argument applied.

As per **claim 2**, Kabenjian discloses "The context based DMA of claim 1,"**[see rejection to claim 1 above]**, further comprising a central parameter store **(register blocks 1 to 4 in fig.2)** for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports **(see col. 8, lines 45-60)**.

As per **claim 3**, Kabenjian discloses wherein the direct memory access controller further comprises means for servicing the request **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**, comprising: means for queuing a memory operation **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**; means for updating parameters **(see Col. 11, lines 29-31)**; and means for fetching and storing parameters in the central parameter store **(see fig. 4 and col. 3, lines 20-52)**.

As per **claim 4**, Kabenjian discloses an apparatus for communicating data among devices interconnected by a shared a shared access memory **(memory 120)**, comprising; a single DMA controller **(DMA controller 202 in fig. 1)**; in a first device, means for writing data to the memory using the DMA controller; in a second device, means for reading data from the memory using the DMA controller **(see fig. 1 and col. 8, lines 45-60)**; wherein the DMA controller receives information from a DMA context memory specifying parameters for writing data from the first device to the memory **(see fig. 1 and col. 8, lines 45-60)**, and wherein the DMA controller is adapted to enable simultaneous reading and writing memory access operations **(col. 7, lines 6-12 discloses "The CPU bus 105, the memory bus 110, the primary I/O bus 152, and the secondary I/O bus 182 can operate independently so that various combinations of the above-described data transfers can occur simultaneously. For example, an access of the memory unit 120 by the CPU 100 over the CPU bus 105 and the memory bus 110 can occur simultaneously with a data transfer between the DMA unit 200 and a device on the primary I/O bus 152, using the primary I/O bus 152")**.

As per **claims 5 and 6**, Kabenjian discloses: a buffer control unit for communicating to the DMA controller an indication of an amount of data written into the memory by the first device through the DMA controller and for communicating to the DMA controller an indication of the amount of data read from the memory by the second device through the DMA controller **(see fig. 4 and col. 8, lines 45-60)**; and wherein the DMA controller reads/write data from/to the memory for the second device if data is available as determined by the indicated amount of data

written to the memory and the amount of data read from the memory as communicated by the buffer control unit **(see fig. 1 and col. 8, lines 45-60)**.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

2. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated August 11, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-6** are rejected under 35 U.S.C. 102(b) as being anticipated by Kabenjian (US pat. 5,613,162).

5. As per **claim 1**, Kabenjian discloses "1. A context based direct memory access architecture **(computer system 90 of fig. 1)**, comprising: a memory **(memory 120)**; a plurality of ports **(the I/O access point of the multiple devices, such as controller 154, 160, 162, and 166 in fig. 1. As also discloses in col. 6, lines 37-41, "The architecture of the computer system 90 can also be implemented to allow data transfers between a first device on the primary I/O bus 152, such as the LAN controller 166 and a second device on the primary I/O bus 152, such as the graphics controller 160, using the primary I/O bus 152.")**, wherein each port has an associated buffer for temporarily storing data transferred through the port, and wherein each port has an associated direct memory access channel **(col. 8, lines 45-60 discloses "The DMA unit 200 of the preferred embodiment has four independent DMA channels. A first DMA channel comprises the first register block 300 and the first data buffer 252. A second DMA channel comprises the second register block 320 and the second data buffer 254. A third DMA channel comprises the third register block 340 and the third data buffer 256. A fourth DMA channel comprises the fourth register block 360 and the fourth data buffer 258. Each DMA channel in the DMA unit 200 is preferably used for DMA transfers with a particular I/O device or a particular group of I/O devices. For example, the first**

DMA channel may be used with the IDE controller 154, the second DMA channel may be used with the graphics controller 160, the third DMA channel may be used with the SCSI controller 162, and the fourth DMA channel may be used with the LAN controller 166"); a direct memory access controller **(DMA controller 202 in fig. 1)** that receives requests for accessing the memory by the plurality of ports **(see fig. 1 and col. 11, lines 22-30)**, wherein each request is received from one of the plurality of ports **(see fig. 1 and col. 11, lines 22-30)**, and wherein the direct memory access controller stores parameters defining the direct memory access operations for each port **(see fig. 4 and col. 13, lines 10-17, which discloses "In the preferred embodiment, the I/O device parameter registers are loaded by the system basic input/output system (BIOS) during system initialization because at that time it will be known which I/O devices are present and which DMA channels are dedicated to particular I/O resources. Thus, the values in the I/O parameter registers are selected to adapt the timing of the DMA transfers to the data transfer characteristics of the I/O device."**), and wherein after a request is received from a port the direct memory access controller loads the parameters for the current direct memory access operation for the port to enable the port to access the memory **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**.

6. As per **claim 2**, Kabenjian discloses "The context based DMA of claim 1,"**[see rejection to claim 1 above]**, further comprising a central parameter store **(register blocks 1 to 4 in fig.2)**

for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports **(see col. 8, lines 45-60)**.

7. As per **claim 3**, Kabenjian discloses wherein the direct memory access controller further comprises means for servicing the request **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**, comprising: means for queuing a memory operation **(see fig. 4 and col. 3, lines 20-52. Col. 11, lines 29-31 also discloses "The DMA controller 202 keeps track of each DMA transfer requested to ensure that each DMA transfer is completed")**; means for updating parameters **(see Col. 11, lines 29-31)**; and means for fetching and storing parameters in the central parameter store **(see fig. 4 and col. 3, lines 20-52).**

8. As per **claim 4**, Kabenjian discloses an apparatus for communicating data among devices interconnected by a shared a shared access memory **(memory 120)**, comprising; a single DMA controller **(DMA controller 202 in fig. 1)**; in a first device, means for writing data to the memory using the DMA controller; in a second device, means for reading data from the memory using the DMA controller **(see fig. 1 and col. 8, lines 45-60)**; wherein the DMA controller receives information from a DMA context memory specifying parameters for writing data from the first device to the memory **(see fig. 1 and col. 8, lines 45-60)**, and wherein the DMA controller is adapted to enable simultaneous reading and writing memory access operations **(col. 7, lines 6-12 discloses "The CPU bus 105, the memory bus 110, the primary I/O bus 152,**

and the secondary I/O bus 182 can operate independently so that various combinations of the above-described data transfers can occur simultaneously. For example, an access of the memory unit 120 by the CPU 100 over the CPU bus 105 and the memory bus 110 can occur simultaneously with a data transfer between the DMA unit 200 and a device on the primary I/O bus 152, using the primary I/O bus 152").

9. As per **claims 5 and 6**, Kabenjian discloses: a buffer control unit for communicating to the DMA controller an indication of an amount of data written into the memory by the first device through the DMA controller and for communicating to the DMA controller an indication of the amount of data read from the memory by the second device through the DMA controller **(see fig. 4 and col. 8, lines 45-60)**; and wherein the DMA controller reads/write data from/to the memory for the second device if data is available as determined by the indicated amount of data written to the memory and the amount of data read from the memory as communicated by the buffer control unit **(see fig. 1 and col. 8, lines 45-60)**.

V. RELEVANT ART CITED BY THE EXAMINER

10. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(c).

11. The following references teach an apparatus for communicating data among devices interconnected by a shared a shared access memory.

U.S. PATENT NUMBER

US 20050188120
US 20040177225
US 6,941,390
US 6,622,181
US 5,634,076

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

12. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

13. Per the instant office action, claims 1-6 have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

15. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Fritz M. Fleming, can be reached at the following telephone number: Area Code (571) 272-4145.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 03, 2006

Ernest Unelus
Examiner
Art Unit 2181

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10/5/2006